Release Notes
Haswell CPU Reference Code
Version 1.9.0

Introduction

Product: Shark Bay Haswell CPU Reference Code
Developed by: Intel Corporation
Software version released date: <11/6/2014>.

NOTE: This document is cumulative and includes information on previous versions. The version information is presented with the newest release first and then regressing through earlier versions.

Purpose of Shark Bay CPU Reference Code

This is sample reference code for core initialization of Haswell Processor. It complies with Haswell Processor BIOS Writer's Guide (BWG) for all programming requirements.

The Processor Reference Code is intended for use as part of Intel BIOS. An OEM may need to modify the code to meet specific platform designs, error handling features, platform specific BIOS features, or other local requirements.

Target Customers

The Haswell CPU reference code is compatible with both mobile and desktop products.

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Version Release History

Version	Description	Release Date
0.7.0	Beta Release	September, 2012
0.7.1	Beta Release	October, 2012
0.8.0	Beta Release	November, 2012
0.8.1	Beta Release	December, 2012
0.9.0	PC Release	January, 2013
1.0.0	PV Release	January, 2013
1.1.0	PV Release	February, 2013
1.2.0	PV Release	February, 2013
1.3.0	PV Release	March, 2013
1.4.0	PV Release	April, 2013
1.5.0	PV Release	May, 2013
1.6.0	PV Release	June, 2013
1.6.1	PV Release	July, 2013
1.6.2	PV Release	August, 2013
1.7.0	PV Release	November, 2013
1.8.0	PV Release	March, 2014
1.9.0	PV Release	November, 2014

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Note: Haswell pre-production/engineering stepping have not been validated with this release of this CPU Reference Code. The reference code will not block the use of these stepping; however, platforms using these stepping may experience unexpected behaviors, including system hangs. To avoid potential issues with these parts, customer should use at least pre-QS samples for their validation.

New Features in Version 1.9.0

1.	N/A

Fixed Bugs in Version 1.9.0

1.	Unsigned PFAT scripts must not be allowed to be accepted via the runtime SMI interface Cpu/BiosGuard/Smm/BiosGuardServices.c Cpu/BiosGuard/Smm/BiosGuardServices.h Cpu/Include/BiosGuardDefinitions.h SampleCode/PolicyInit/Pei/CpuPolicyInitPei.c

Known Issues

N/A

Related Documents

- **Intel Haswell Processor Reference Code Specification_1.9.0.pdf**

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Version 1.8.0

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New Features in Version 1.8.0

2.	Custom TDP Brand string workaround must be removed when CTDP enabled in BIOS. The workaround added to fix brand string issue is causing frequency miscalculations in Win7/Win8. Cpu/PowerManagement/Dxe/PowerLimits.c

Fixed Bugs in Version 1.8.0

2.	PL1 Mailbox Configuration register is not restored at S3 resume. Cpu/PowerManagement/Dxe/Thermal.c

Known Issues

N/A

Related Documents

- **Intel Haswell Processor Reference Code Specification_1.8.0.pdf**

Version 1.7.0

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New Features in Version 1.7.0

3.	Support P-state Limiting on CPPC Systems Cpu\PowerManagement\AcpiTables\Ssdt\Ctdp.asl The ACPI Reference Code also contains updates to support this feature

Fixed Bugs in Version 1.7.0

3.	TXT getsec SENTER fails with PFAT enabled Cpu\CpuInit\Dxe\MpService.c Cpu\Protocol\CpuPlatformPolicy\CpuPlatformPolicy.h

Known Issues

N/A

Related Documents

- **Intel Haswell Processor Reference Code Specification_1.7.0.pdf**

Version 1.6.2

Note: Haswell pre-production/engineering stepping have not been validated with this release of this CPU Reference Code. The reference code will not block the use of these stepping; however, platforms using these stepping may experience unexpected behaviors, including system hangs. To avoid potential issues with these parts, customer should use at least pre-QS samples for their validation.

Fixed Bugs in Version 1.6.2

1.	Add MSR 615h PLATFORM _POWER_LIMIT in mMsrValues[] for S3 save/restore Cpu\PowerManagement\Smm\PowerMgmtS3.c
2.	Update PL3 time windows for mMilliSecondsToMsrValueMapTable setting Cpu\PowerManagement\Dxe\MiscFunctions.c

Known Issues

N/A

Related Documents

- **Intel Haswell Processor Reference Code Specification_1.6.2.pdf**

Version 1.6.1

Note: Haswell pre-production/engineering stepping have not been validated with this release of this CPU Reference Code. The reference code will not block the use of these stepping; however, platforms using these stepping may experience unexpected behaviors, including system hangs. To avoid potential issues with these parts, customer should use at least pre-QS samples for their validation.

New Features in Version 1.6.1

1.	Support P-state Limiting on CPPC Systems Cpu\PowerManagement\AcpiTables\Ssdt\Ctdp.asl The ACPI Reference Code also contains updates to support this feature

Fixed Bugs in Version 1.6.1

1.	Add cold reset when enabling SVID or FIVR faults Cpu/CpuInit/Pei/CpuOcInit.c
2.	MCHBAR + 0x59A0 value is not restored properly after S3 resume. Cpu/PowerManagement/Dxe/Thermal.c
3.	Updated TIME_WINDOW_FIELD programming flow Cpu/PowerManagement/Dxe/MiscFunctions.c Cpu/PowerManagement/Dxe/PowerLimits.c Cpu/PowerManagement/Dxe/PowerMgmtCommon.h
4.	Updated P-State Table for HSW 28W U-Processors Cpu/PowerManagement/Dxe/PowerLimits.c
5.	cTDP-Down has wrong PL1 in MMIO on HSW Y-Processor Cpu/PowerManagement/Dxe/Thermal.c

Known Issues

N/A

Related Documents

- **Intel Haswell Processor Reference Code Specification_1.6.1.pdf**

Version 1.6.0

Note: Haswell pre-production/engineering stepping have not been validated with this release of this CPU Reference Code. The reference code will not block the use of these stepping; however, platforms using these stepping may experience unexpected behaviors, including system hangs. To avoid potential issues with these parts, customer should use at least pre-QS samples for their validation.

New Features in Version 1.6.0

1.	Remove support for Run Busy Bit for MSR_RFI_TUNING (0xE3). Cpu/Include/CpuRegs.h Cpu/PowerManagement/Smm/PowerMgmtS3

Fixed Bugs in Version 1.6.0

1.	Added support for Controllable TDP on Celeron U Processors Cpu\PowerManagement\Dxe\PerformanceStates.c Cpu\PowerManagement\Dxe\PowerLimits.c Cpu\PowerManagement\Dxe\PowerMgmtCommon.h Cpu\PowerManagement\Dxe\PowerMgmtDxe.inf Cpu\PowerManagement\Dxe\PowerMgmtInit.c

Known Issues

N/A

Related Documents

- **Intel Haswell Processor Reference Code Specification_1.6.0.pdf**

Version 1.5.0

Note: Haswell pre-production/engineering stepping have not been validated with this release of this CPU Reference Code. The reference code will not block the use of these stepping; however, platforms using these stepping may experience unexpected behaviors, including system hangs. To avoid potential issues with these parts, customer should use at least pre-QS samples for their validation.

New Features in Version 1.5.0

1.	Addition of new PL1 features on Haswell - IA Core Cpu\PowerManagement\Dxe\PowerMgmtCommon.h Cpu\PowerManagement\Dxe\PowerMgmtInit.c Cpu\PowerManagement\Dxe\Thermal.c Cpu\Protocol\CpuPlatformPolicy\CpuPlatformPolicy.h Cpu\Protocol\CpuPlatformPolicy\CpuPmConfig.h Cpu\SampleCode\CpuPolicyInit\Dxe\CpuPolicyInitDxe.c
2.	Update Reset type as Warm Boot for HT and Active Core strapping change Cpu/CpuInit/Pei/CpuInitPeim.c
3.	Creating SampleCode for Boot Guard TPM EventLog Creation Cpu\SampleCode\Library\BootGuardTpmEventLogLib\BootGuardTpmEventLogLib.c Cpu\SampleCode\Library\BootGuardTpmEventLogLib\BootGuardTpmEventLogLib.h
4.	BIOS PL1 Override 41W for 47W 2C processors SKU Cpu\Include\CpuRegs.h Cpu\PowerManagement\Dxe\PowerLimits.c Cpu\PowerManagement\Dxe\PowerMgmtCommon.h Cpu\PowerManagement\Dxe\PowerMgmtInit.c
5.	BIOS OC: Set cTDP Disabled's MMIO values for PL1/2 to 0, to enable overclocking via MSR Cpu\Include\PowerMgmtDefinitions.h Cpu\PowerManagement\Dxe\PowerLimits.c

Fixed Bugs in Version 1.5.0

1.	PL1 thermal throttling setup option enable, disables the feature Cpu\PowerManagement\Dxe\Thermal.c
2.	InitPl1ThermalControl code should apply to general HSW and CRW Cpu\PowerManagement\Dxe\Thermal.c
3.	S3 Resume hang at PC 0xE3 with Win8 UEFI install + CSM Enable Cpu\CpuInit\Dxe\MpCommon.c

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Known Issues

N/A

Related Documents

- **Intel Haswell Processor Reference Code Specification_1.5.0.pdf**

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Version 1.4.0

Note: Haswell pre-production/engineering stepping have not been validated with this release of this CPU Reference Code. The reference code will not block the use of these stepping; however, platforms using these stepping may experience unexpected behaviors, including system hangs. To avoid potential issues with these parts, customer should use at least pre-QS samples for their validation.

New Features in Version 1.4.0

1.	Bit 31 of PCH's PMSYNC_TPR_CFG should be set to lock the register Cpu\PowerManagement\Dxe\MiscFunctions.c
2.	System BIOS must set power limit clamp bit on all HSW/BDW parts Cpu\PowerManagement\Dxe\Thermal.c
3.	C_STATE_LATENCY_CONTROL_1 register programing needs to be updated Cpu\Include\PowerMgmtDefinitions.h

Fixed Bugs in Version 1.4.0

1.	Allocate memory for the mCpuPmConfig.ThermalFuncEnables in sample code Cpu\SampleCode\CpuPolicyInit\Dxe\CpuPolicyInitDxe.c
2.	BIOS doesn't populate the Processor Upgrade property of Processor Information (Type 4) Cpu\SampleCode\CpuPolicyInit\Dxe\CpuPolicyInitDxe.c

Known Issues

N/A

Related Documents

- **Intel Haswell Processor Reference Code Specification_1.4.0.pdf**

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Version 1.3.0

Note: Haswell pre-production/engineering stepping have not been validated with this release of this CPU Reference Code. The reference code will not block the use of these stepping; however, platforms using these stepping may experience unexpected behaviors, including system hangs. To avoid potential issues with these parts, customer should use at least pre-QS samples for their validation.

Fixed Bugs in Version 1.3.0

1.	OS never makes any P-state requests/always runs at 8x and BIOS programs erroneous ConfigTDP value when ConfigTDP disabled Cpu\PowerManagement\Dxe\PowerLimits.c
2.	BIOS is corrupting the page that is reserved by OS kernel on wake from S3 Cpu\CpuInit\Dxe\MpCommon.c
3.	IVR BIOS SSC function does not work Cpu\CpuInit\Pei\CpuInitPeim.c

Known Issues

N/A

Related Documents

- **Intel Haswell Processor Reference Code Specification_1.3.0.pdf**

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Version 1.2.0

Note: Haswell pre-production/engineering stepping have not been validated with this release of this CPU Reference Code. The reference code will not block the use of these stepping; however, platforms using these stepping may experience unexpected behaviors, including system hangs. To avoid potential issues with these parts, customer should use at least pre-QS samples for their validation.

New Features in Version 1.2.0

1.	Update CPU RC PPI revision for AnC policy changes Cpu\CpuInit\Pei\BootGuardInit.c Cpu\Ppi\CpuPlatformPolicy\CpuPlatformPolicy.h
2.	Setup Custom CTDP menu to accept the fractional PL1 and PL2 values Cpu\PowerManagement\Dxe\PowerMgmtInit.c - Cpu\Protocol\CpuPlatformPolicy\CpuPmConfig.h - Cpu\SampleCode\CpuPolicyInit\Dxe\CpuPolicyInitDxe.c

Fixed Bugs in Version 1.2.0

1.	Turbo Ratio Limit not restored on S3 resume Cpu\PowerManagement\Smm\PowerMgmtS3.c
2.	PL1 value is not programmed correctly on 11.5W sku when Ctdp Nominal Selected. Cpu\PowerManagement\Dxe\PerformanceStates.c Cpu\PowerManagement\Dxe\PowerLimits.c Cpu\PowerManagement\Dxe\PowerMgmtCommon.h Cpu\PowerManagement\Dxe\PowerMgmtInit.c Cpu\PowerManagement\Dxe\Thermal.c
3.	Low TDP power limit value observed “Zero” from DPTF power option window Cpu\PowerManagement\Dxe\PerformanceStates.c Cpu\PowerManagement\Dxe\PowerLimits.c Cpu\PowerManagement\Dxe\PowerMgmtCommon.h Cpu\PowerManagement\Dxe\PowerMgmtInit.c Cpu\PowerManagement\Dxe\Thermal.c
4.	Max P-state value is set to match the BIOS-specified 1-core Turbo multiplier Cpu\PowerManagement\Dxe\PerformanceStates.c

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Known Issues

N/A

Related Documents

- **Intel Haswell Processor Reference Code Specification_1.2.0.pdf**

Release Notes
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Version 1.1.0

Note: Haswell pre-production/engineering stepping have not been validated with this release of this CPU Reference Code. The reference code will not block the use of these stepping; however, platforms using these stepping may experience unexpected behaviors, including system hangs. To avoid potential issues with these parts, customer should use at least pre-QS samples for their validation.

New Features in Version 1.1.0

1.	Change in Power Limit 2 BIOS overrides for HSW ULT Cpu\PowerManagement\Dxe\PowerLimits.c Cpu\PowerManagement\Dxe\PowerMgmtCommon.h Cpu\PowerManagement\Dxe\PowerMgmtInit.c
2.	Anchor Cove PPI policy name change to “Boot Guard”, requires platform code update to reflect “Boot Guard” and integrate this RC version 1.1.0
3.	Default 'PowerLimit1 Thermal Throttling' is Enabled on ULX and disabled on other processors Cpu\PowerManagement\Dxe\Thermal.c
4.	Update ULT PCH power level programming Cpu\Include\Library\CpuPlatformLib.h Cpu\PowerManagement\Dxe\MiscFunctions.c Cpu\PowerManagement\Dxe\PowerMgmtCommon.h Pch\Include\PchRegs\PchRegsRcrb.h – PCH Reference Code

Fixed Bugs in Version 1.1.0

1.	FIVR BIOS Bug for setting " RFI Freq. Tuning offset" Cpu\PowerManagement\Dxe\MiscFunctions.c
2.	PL3 customer parameters cannot be set on C0 HSW. Cpu\PowerManagement\Dxe\PowerLimits.c
3.	System does not cold reset when attempting to re-enable FIVR faults or SVID Support Cpu\CpuInit\Pei\CpuOcInit.c
4.	Update HSW ULT 24 MHz calibration code Cpu\Include\Library\CpuPlatformLib.h Cpu\PowerManagement\Dxe\IdleStates.c
5.	CPU Package C states always stays at C3 after changing calibrate 24MHz BCLK to BIOS Cpu\Include\Library\CpuPlatformLib.h Cpu\PowerManagement\Dxe\IdleStates.c

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Known Issues

N/A

Related Documents

- **Intel Haswell Processor Reference Code Specification_1.1.0.pdf**

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Version 1.0.0

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New Features in Version 1.0.0

1.	BIOS must implement RING_RATIO_LIMIT MSR 0x620 Cpu\Include\CpuRegs.h Cpu\CpuInit\Pei\CpuInitPeim.c
2.	Default Tau Value for MSR 610h 23:17 should be programmed to 8 seconds (0001101) for all Desktop processors Cpu\Include\PowerMgmtDefinitions.h

Fixed Bugs in Version 1.0.0

1.	BIOS should not use MMIO PL1 overrides for 15W Sku Cpu\PowerManagement\Dxe\PowerLimits.c

Known Issues

N/A

Related Documents

- **Intel Haswell Processor Reference Code Specification_1.0.0.pdf**

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Version 0.9.0

Note: HSW A0 stepping is not supported with this release of Haswell CPU reference code due to no validation is performed with A0 stepping. However, it will not block use of HSW A0. Thus, no A0 specific fix is implemented for this release.

New Features in Version 0.9.0

1.	BIOS must implement RING_RATIO_LIMIT MSR 0x620 \Cpu\Include\CpuRegs.h \Cpu\CpuInit\Pei\CpuInitPeim.c

Fixed Bugs in Version 0.9.0

1.	Instead of clipping the bits 29:28,Change code to use max value 15c when user selects value greater than 15c and 6 bits Tcc offset is not supported. \Cpu\CpuInit\Pei\CpuInitPeim.c
2.	Wrong lock used in CPU Reference Code, MSR_TURBO_ACTIVATION_RATIO_LOCK should be used instead of CONFIG_TDP_CONTROL_LOCK \Cpu\PowerManagement\Dxe\PowerLimits.c

Known Issues

N/A

Related Documents

- **Intel Haswell Processor Reference Code Specification_0.9.0.pdf**

Release Notes
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Version 0.8.1

Note: HSW A0 stepping is not supported with this release of Haswell CPU reference code due to no validation is performed with A0 stepping. However, it will not block use of HSW A0. Thus, no A0 specific fix is implemented for this release.

New Features in Version 0.8.1

1.	Added support for BIOS configuration of PL3 \Cpu\CpuInit\Dxe\CpuInitDxe.c \Cpu\Include\CpuRegs.h \Cpu\PowerManagement\Dxe\MiscFunctions.c \Cpu\PowerManagement\Dxe\PowerLimits.c \Cpu\PowerManagement\Dxe\PowerMgmtCommon.h \Cpu\PowerManagement\Dxe\PowerMgmtInit.c \Cpu\Protocol\CpuPlatformPolicy\CpuPmConfig.h \Cpu\SampleCode\CpuPolicyInit\Dxe\CpuPolicyInitDxe.c

Fixed Bugs in Version 0.8.1

1.	Fixed issue in which the CPU policy value/pointer in S3 resume path (CpuS3Peim.c) is incorrect. The CPU_CONFIG_PPI still points to cache, not final pointer in memory. \Cpu\CpuS3\Pei\CpuS3Peim.c \Cpu\Ppi\CpuPlatformPolicy\CpuPlatformPolicy.h \Cpu\SampleCode\CpuPolicyInit\Pei\CpuPolicyInitPei.c
2.	For ULT 15W HSW SKU the recommended PL2 setting is 25W. So it is expected for PL1=PL2=25W in these configurations. PPCC needs to be updated to report the correct PL1 and PL2 values as provided by the PPM code. cTDP-Down – PL2 = 25W cTDP-Nominal – PL2 = 25W cTDP-Up – PL2 = 25W \Cpu\PowerManagement\Dxe\PowerLimits.c
3.	Create individual timer event "CheckThisAPEvent" for each logical processor \Cpu\CpuInit\Dxe\MpService.c \Cpu\CpuInit\Dxe\MpService.h

4.	Fixed bug in which SSDT ACPI table does not build for Lake Tiny \Cpu\Include\CpuPowerMgmt.dsc
5.	Fixed bug in which system does not cold reset when attempting to re-enable FIVR faults or SVID Support \Cpu\CpuInit\Pei\CpuOcInit.c
6.	Fixed bug in which cTDP brandstring reports incorrect CPU frequency \Cpu\PowerManagement\Dxe\PowerLimits.c \Cpu\PowerManagement\Dxe\PowerMgmtInit.c
7.	Fixed bug in which the Turbo P state P0 is Non Turbo frequency +100Mz,it should be Non Turbo frequency Non Turbo frequency +1Mz. \Cpu\PowerManagement\Dxe\PerformanceStates.c \Cpu\PowerManagement\Dxe\PowerLimits.c

Known Issues

N/A

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Version 0.8.0

Note: HSW A0 stepping is not supported with this release of Haswell CPU reference code due to no validation is performed with A0 stepping. However, it will not block use of HSW A0. Thus, no A0 specific fix is implemented for this release.

New Features in Version 0.8.0

1.	BIOS implementation of FIVR RFI/EMI tuning
2.	Add Anchor Cove Configuration to Security policy PPI

Fixed Bugs in Version 0.8.0

1.	Updated interface and data addresses for 24Mhz BCLK PCODE mailbox \Cpu\Ppi\CpuPlatformPolicy\CpuPlatformPolicy.h \Cpu\PowerManagement\Dxe\IdleStates.c
2.	Fixed issue in which code was programming IntendCoreFrequency = “Maximum Non Turbo Ratio”, and it goes to "current speed" field in SMBIOS type4. \Cpu\CpuInit\Dxe\MpCommon.c \Cpu\Include\CpuRegs.h \CpuPolicyInit\Dxe\CpuPolicyInitDxe.c
3.	Fix of the S3 resume hang (PC 0x0055) issue caused by the wrong addresses within the Memory Write Boot Script items. \Cpu\PowerManagement\Dxe\MiscFunctions.c
4.	Fix issue in which SMM THUNK driver has problem causing it not to return when call into thunk code and moved SMM Thunk driver to sample code \SampleCode\SmmThunk\Smm\SmmThunkDriver.c \SampleCode\SmmThunk\
5.	Fixed issue in which Package C6 was not occurring, increased the C-6 latency \Cpu\Include\PowerMgmtDefinitions.h

Known Issues

N/A

Related Documents

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